International Journal of Engineering Science and Advanced Technology (IJESAT)
Vol 26 Issue 4(1) (April) 2026
Received: 10-2-2026 Accepted: 17-3-2026 Published: 16-4-2026

Design and HSPICE Analysis of an Novel Approximate Full Adder

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ABSTRACT: This paper presents the design of an 8-transistor (8T) approximate full adder using pass transistor logic (PTL) in 32 nm CMOS technology, targeting low-power and high-speed applications. By reducing the transistor count and simplifying the conventional full adder structure, the proposed design achieves significant improvements in power consumption, delay, and area. The approximation in Sum and Carry outputs enables an efficient trade-off between accuracy and performance, making it suitable for error-tolerant applications such as image processing and multimedia systems. The circuit is designed and simulated using HSPICE, and its performance is evaluated in terms of power dissipation, propagation delay, and power-delay product (PDP). Simulation results indicate that the proposed 8T design offers superior energy efficiency compared to conventional full adders while maintaining acceptable error characteristics for practical applications.

Keywords: Approximate Full Adder, 8T Design, Pass Transistor Logic (PTL), 32 nm CMOS Technology, Low Power VLSI, Energy Efficiency, HSPICE Simulation, Propagation Delay, Power-Delay Product (PDP), Error-Tolerant Computing, Image Processing Applications

I. Introduction

The increasing demand for energy-efficient and high-performance digital systems has driven significant research in low-power VLSI design, particularly for applications such as image processing, multimedia, and machine learning. In these domains, exact computation is not always necessary, as minor errors often have negligible impact on the overall output quality. This observation has led to the emergence of approximate computing, a design paradigm that intentionally relaxes computational accuracy to achieve substantial improvements in power consumption, speed, and silicon area. Among the fundamental arithmetic circuits, the full adder plays a crucial role in the implementation of complex components such as multipliers and accumulators, making its optimization highly important. Conventional full adder designs typically require a large number of transistors, resulting in higher power dissipation and increased delay. To address these limitations, approximate full adders with reduced transistor counts have been proposed.

In particular, the 8-transistor (8T) approximate full adder has gained attention due to its compact structure and energy-efficient operation. By simplifying the logic functions of Sum and Carry outputs, the 8T design significantly reduces switching activity and parasitic capacitances. Furthermore, pass transistor logic (PTL) offers an effective approach to minimize transistor usage by eliminating redundant components and utilizing fewer logic levels compared to traditional CMOS logic. When implemented in advanced technologies such as 32 nm CMOS, PTL-based designs can achieve enhanced performance in terms of speed and power efficiency. However, these benefits come at the cost of reduced signal integrity and potential computational inaccuracies, which must be carefully analyzed.

In this work, an 8T approximate full adder based on PTL is designed and simulated using HSPICE in 32 nm technology. The proposed design focuses on achieving an optimal balance between accuracy and hardware efficiency. Its performance is evaluated in terms of power consumption, propagation delay, and power-delay product, demonstrating its suitability for error-resilient applications like image processing systems.

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II. Related Background

The design of energy-efficient arithmetic circuits has become a key research focus in modern VLSI systems due to the rapid growth of portable and high-performance electronic devices. Among these circuits, the full adder serves as a fundamental building block in arithmetic units such as multipliers, adders, and digital signal processors. Traditional full adder designs based on complementary CMOS logic typically require 20–28 transistors, leading to increased power consumption, propagation delay, and silicon area, which are critical constraints in nanoscale technologies.

To overcome these limitations, researchers have explored alternative design techniques such as transmission gate logic, pass transistor logic (PTL), and hybrid logic styles. PTL, in particular, has gained significant attention due to its ability to reduce transistor count and minimize capacitive loading by allowing signals to pass directly through transistors. This results in faster switching speeds and lower dynamic power consumption. However, PTL designs often suffer from threshold voltage drop and reduced output voltage swing, which can affect reliability in deep submicron technologies. With the advancement of technology scaling into the nanometer regime, such as 32 nm CMOS, leakage power and short-channel effects have become dominant concerns. These challenges necessitate innovative circuit design approaches that can maintain performance while minimizing energy consumption. In this context, approximate computing has emerged as an effective solution for error-resilient applications. By allowing controlled inaccuracies in computation, approximate circuits significantly improve energy efficiency and reduce hardware complexity.

Approximate full adders are specifically designed to exploit this concept by simplifying the logic expressions of Sum and Carry outputs. Various designs such as 10T, 12T, and even lower transistor-count adders have been proposed in the literature, each offering different trade-offs between accuracy and performance. Among them, the 8T approximate full adder stands out due to its minimal transistor usage and compact structure, making it highly suitable for large-scale integration. In many approximate designs, the Carry output is prioritized for accuracy, as it has a greater impact on overall arithmetic operations, while the Sum output is approximated to reduce complexity. Error metrics such as Mean Error Distance (MED), Mean Absolute Error (MAE), and Normalized Error Distance (NED) are commonly used to evaluate the performance of these designs.

Additionally, parameters such as power consumption, propagation delay, and power-delay product (PDP) are used to assess circuit efficiency. Simulation tools like HSPICE play a crucial role in analyzing the performance of these circuits under different operating conditions and process variations. By implementing approximate full adders in advanced CMOS technologies using PTL, designers can achieve a desirable balance between accuracy, power efficiency, and speed. This makes such designs highly applicable in image processing, multimedia systems, and other applications where slight computational errors are acceptable in exchange for significant hardware benefits.

III. Proposed Method

In this work, an 8-transistor (8T) approximate full adder is designed using pass transistor logic (PTL) in 32 nm CMOS technology to achieve low power consumption, reduced delay, and minimal area. The proposed design focuses on simplifying the conventional full adder structure by reducing the number of transistors and approximating the logic functions of the Sum and Carry outputs. PTL is employed to efficiently implement logic functions with fewer devices, thereby reducing switching activity and parasitic capacitances.

The proposed adder utilizes a compact PTL-based structure where the Sum output is approximated as $A \oplus B$, effectively ignoring or partially considering the carry input (Cin) to reduce circuit complexity. The Carry output is implemented using a simplified logic expression, typically prioritizing dominant input combinations such as $A \cdot B$ and $B \cdot Cin$, ensuring that the most significant carry conditions are preserved. This selective approximation helps maintain acceptable accuracy while significantly improving energy efficiency.

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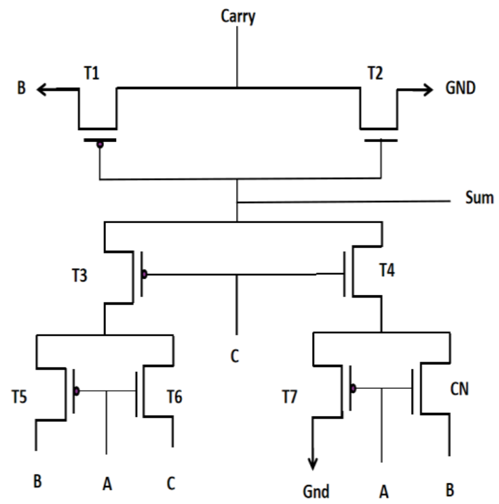

Fig. 1. Proposed Approximate Full Adder

TABLE. 1 Proposed Approximate Full Adder

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

The circuit is designed at the transistor level using NMOS-based pass transistor configurations, with careful consideration of threshold voltage drop and signal degradation issues commonly associated with PTL. To mitigate these effects, proper transistor sizing and minimal buffering techniques are incorporated. The design is simulated using HSPICE in a 32 nm technology environment under various input combinations and supply voltage conditions.Performance evaluation is carried out in terms of power consumption, propagation delay, and power-delay product (PDP). Additionally, the accuracy of the proposed adder is analyzed using error metrics such as Mean Error Distance (MED) and Normalized Error Distance (NED). The results are compared with conventional CMOS and other approximate full adder designs to demonstrate the effectiveness of the proposed method. The compact structure and improved energy efficiency make the proposed 8T approximate full adder highly suitable for integration in error-tolerant applications such as image processing and digital signal processing systems.

IV. Results and Discussion

The proposed 8T approximate full adder designed using pass transistor logic (PTL) in 32 nm CMOS technology was simulated using HSPICE to evaluate its performance. The results demonstrate a significant reduction in power consumption compared to conventional CMOS full adders due to the lower transistor count and reduced switching activity. The simplified structure also contributes to a decrease in propagation delay, resulting in faster operation. Consequently, the power-delay product (PDP) of the proposed design is considerably improved, indicating higher energy efficiency. The circuit was tested under various input combinations and supply voltage levels to ensure stable operation. Although the design introduces approximation in the Sum and Carry outputs, the observed errors are limited and acceptable for error-resilient applications.

Error analysis using metrics such as Mean Error Distance (MED) and Normalized Error Distance (NED) shows that the deviation from exact computation remains within tolerable limits. A comparative analysis with existing full adder designs, including conventional CMOS and other approximate adders (such as 10T and 12T structures), reveals that the proposed 8T design achieves superior performance in terms of power savings and area efficiency, with only a marginal compromise in accuracy. These results confirm that the proposed design is well-suited for applications like image processing and multimedia systems, where energy efficiency is more critical than exact precision.

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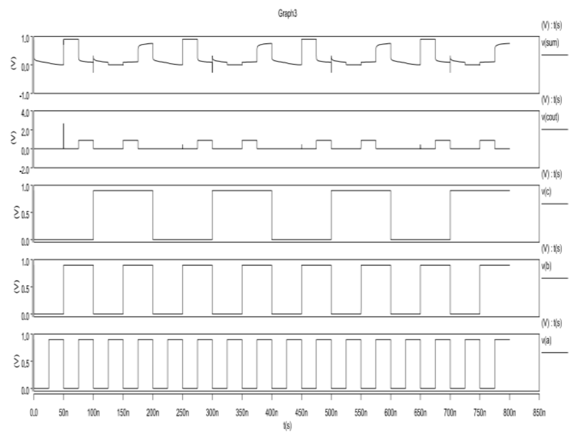

Fig. 2. Output Wave form of Proposed Approximate Full Adder

TABLE. 2. Various parameters of Proposed Approximate Full Adder

PARAMETERS	Output Value
POWER	2.315e-8
DELAY	2.500e-8
POWER DELAY PRODUCT(PDP)	5.787e-16
ENERGY DELAY PRODUCT(EDP)	1.446e-23
ADP	4.741e-30

V. Conclusion

This work presents an efficient design of an **8-transistor (8T) approximate full adder** using **pass transistor logic (PTL)** in **32 nm CMOS technology**. The proposed design significantly reduces transistor count, leading to lower power consumption, reduced propagation delay, and improved power-delay product (PDP). By introducing controlled approximation in the Sum and Carry outputs, the circuit achieves an effective trade-off between accuracy and hardware efficiency. Simulation results obtained using HSPICE confirm that the proposed adder outperforms conventional and existing approximate designs in terms of energy efficiency while maintaining acceptable error levels. Due to its compact structure and enhanced performance, the proposed 8T approximate full adder is highly suitable for integration in error-tolerant applications such as image processing and digital signal processing systems.

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